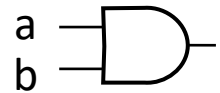
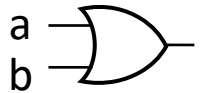
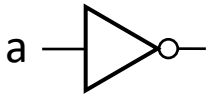
EECS 270 Fall 2022
Introduction to Logic Design

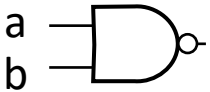
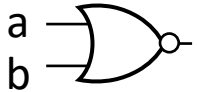
Boolean gates & other common building blocks

Basic Boolean gates

	AND	OR	NOT
Schematic symbol			
Logic symbol	a·b	a+b	a’ or $\overline{a}$
Verilog symbols	&& or &	|| or |	! or ~

Inputs		Outputs		
a	**b**	**a·b**	**a+b**	**$\overline{a}$**
0	0	0	0	1
0	1	0	1	1
1	0	0	1	0
1	1	1	1	0

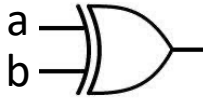
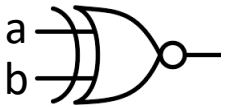
More Boolean gates

	NAND	NOR
Schematic symbol		
Logic symbol	$\overline{a \cdot b}$	$\overline{a+b}$
Verilog expression	~(a&b)	~(a|b)

- NAND returns 1 when AND return 0, and vice versa
- NOR returns 1 when OR returns 0, and vice versa

Inputs		Outputs	
a	**b**	$\overline{a \cdot b}$	$\overline{a+b}$
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

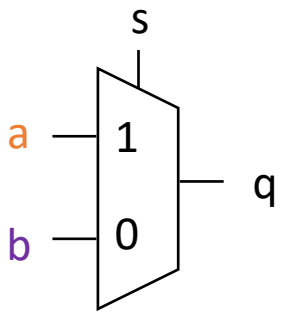
More Boolean gates

	XOR	XNOR
Schematic symbol		
Logic symbol	$a \oplus b$	$\overline{a \oplus b}$
Verilog expression	a^b	~(a^b)

- XOR = $(a + b) \cdot (\overline{a} + \overline{b})$
- XNOR returns 1 when XOR returns 0, and vice versa

Inputs		Outputs	
a	**b**	$\overline{a \oplus b}$	$\overline{a \oplus b}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

2x1 Multiplexer (2:1 MUX)




```
if (s)
    q = a;
else
    q = b;
```

Inputs			Output
s	**a**	**b**	**q**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1